IN THE CLAIMS:

Please cancel claims 6 and 12-22 without prejudice or disclaimer as to the subject matter contained therein.

Please amend the claims as shown in the following claims listing.

1. (Currently amended) An apparatus for adding a first value 'A' and a second value 'B', each including a plurality of bits, wherein bits in corresponding bit positions of said first value and said second value form respective columns, said apparatus comprising:

a plurality of combiner units each configured to provide a generate and propagate bit pair in response to receiving respective bits of said first value and said second value which correspond to a plurality of said respective columns;

a carry creation unit coupled to said plurality of combiner units and configured to create an ordered plurality of carry bits each corresponding to one or more of said generate and propagate bit pairs; and

a plurality of summation units each configured to generate a plurality of sum bits in response to receiving said respective bits of said first value and said second value which correspond to said plurality of said respective columns, wherein a subset of said plurality of summation units is configured to generate a portion of said plurality of sum bits in response to receiving respective ones of said ordered plurality of carry bits;

wherein each of said plurality of combiner units is configured to create a generate bit G_j and a propagate bit P_j using a combinatorial logic circuit to implement a logic function substantially equivalent to

$$Gj = (A_{i+1} \bullet B_{i+1}) + (A_{i+1} \bullet A_i \bullet B_i) + (B_{i+1} \bullet A_i \bullet B_i) \text{ and}$$

$$Pj = (A_{i+1} + B_{i+1}) \bullet (A_i + B_i).$$

2. (Original) The apparatus as recited in claim 1, wherein another subset of said plurality of summation units is configured to generate another portion of said plurality of sum bits in response to receiving a different carry bit.

3. (Original) The apparatus as recited in claim 1, wherein each generate and propagate bit pair occupies an ordered position from a least significant ordered position to a most significant ordered position.

4. (Original) The apparatus as recited in claim 3, wherein each of said ordered plurality of carry bits occupies an ordered position from a least significant ordered position to a most significant ordered position.

5. (Original) The apparatus as recited in claim 4, wherein each of said ordered plurality of carry bits is based upon all generate and propagate bit pairs occupying less significant ordered positions.

6. (Cancelled)

7. (Currently amended) ~~The apparatus as recited in claim 1,~~ An apparatus for adding a first value 'A' and a second value 'B', each including a plurality of bits, wherein bits in corresponding bit positions of said first value and said second value form respective columns, said apparatus comprising:

a plurality of combiner units each configured to provide a generate and propagate bit pair in response to receiving respective bits of said first value and said second value which correspond to a plurality of said respective columns;

a carry creation unit coupled to said plurality of combiner units and configured to create an ordered plurality of carry bits each corresponding to one or more of said generate and propagate bit pairs; and

a plurality of summation units each configured to generate a plurality of sum bits in response to receiving said respective bits of said first value and said second value which correspond to said plurality of said respective columns, wherein a subset of said plurality of summation units is configured to generate a portion of said plurality of sum bits in response to receiving respective ones of said ordered plurality of carry bits;

wherein each of said plurality of summation units is configured to create a sum bit S_i and a sum bit S_{i+1} using a combinatorial logic circuit to implement a logic function substantially equivalent to $S_i = (A_i \oplus B_i) \oplus C_j$ and for $C_j = 0$, then $S_{i+1} = (A_{i+1} \oplus B_{i+1}) \oplus (A_i \bullet B_i)$ and for $C_j = 1$, then $S_{i+1} = (A_{i+1} \oplus B_{i+1}) \oplus (A_i + B_i)$.

8. (Currently amended) ~~The apparatus as recited in claim 1,~~ An apparatus for adding a first value 'A' and a second value 'B', each including a plurality of bits, wherein bits in corresponding bit positions of said first value and said second value form respective columns, said apparatus comprising:

a plurality of combiner units each configured to provide a generate and propagate bit pair in response to receiving respective bits of said first value and said second value which correspond to a plurality of said respective columns;

a carry creation unit coupled to said plurality of combiner units and configured to create an ordered plurality of carry bits each corresponding to one or more of said generate and propagate bit pairs; and

a plurality of summation units each configured to generate a plurality of sum bits in response to receiving said respective bits of said first value and said second value which correspond to said plurality of said respective columns, wherein a subset of said plurality of summation units is configured to generate a portion of said plurality of sum bits in response to receiving respective ones of said ordered plurality of carry bits;

wherein each of said plurality of combiner units is configured to create a generate bit G_j and a propagate bit P_j using a combinatorial logic circuit to implement a logic function substantially equivalent to $Gj = (A_{i+3} \bullet B_{i+3}) + (A_{i+3} \bullet A_{i+2} \bullet A_{i+1} \bullet B_{i+1}) + (B_{i+3} \bullet A_{i+2} \bullet A_{i+1} \bullet B_{i+1})$ and $Pj = (A_{i+3} + B_{i+3}) \bullet (A_{i+1} + B_{i+1}) \bullet (A_{i+2} \bullet A_i)$, and wherein every other bit position of said second value is equal to zero.

9. (Currently amended) ~~The apparatus as recited in claim 1,~~ An apparatus for adding a first value 'A' and a second value 'B', each including a plurality of bits, wherein bits in

corresponding bit positions of said first value and said second value form respective columns, said apparatus comprising:

a plurality of combiner units each configured to provide a generate and propagate bit pair in response to receiving respective bits of said first value and said second value which correspond to a plurality of said respective columns;

a carry creation unit coupled to said plurality of combiner units and configured to create an ordered plurality of carry bits each corresponding to one or more of said generate and propagate bit pairs; and

a plurality of summation units each configured to generate a plurality of sum bits in response to receiving said respective bits of said first value and said second value which correspond to said plurality of said respective columns, wherein a subset of said plurality of summation units is configured to generate a portion of said plurality of sum bits in response to receiving respective ones of said ordered plurality of carry bits;

wherein each of said plurality of summation units is configured to create sum bits S_i, S_{i+1}, S_{i+2} and S_{i+3} using a combinatorial logic circuit to implement a logic function substantially equivalent to $S_i = A_i \oplus C_j$ and for $C_j = 0$, then $S_{i+1} = A_i \oplus B_{i+1}$, $S_{i+2} = (A_{i+1} \bullet B_{i+1}) \oplus A_{i+2}$ and $S_{i+3} = (A_{i+3} \oplus B_{i+3}) \oplus (A_{i+1} \bullet B_{i+1} \bullet A_{i+2})$ and for $C_j = 1$, then $S_{i+1} = (A_{i+1} \oplus B_{i+1}) \oplus A_i$, $S_{i+2} = ((A_{i+1} \bullet B_{i+1}) + (A_i \bullet B_{i+1}) + (A_i \bullet A_{i+1})) \oplus A_{i+2}$ and $S_{i+3} = ((A_{i+1} \bullet B_{i+1} \bullet A_{i+2}) + (A_i \bullet B_{i+1} \bullet A_{i+2}) + (A_i \bullet A_{i+1} \bullet A_{i+2})) \oplus (A_{i+3} \oplus B_{i+3})$, and wherein every other bit position of said second value is equal to zero.

10. (Original) The apparatus as recited in claim 3, wherein said ordered plurality of carry bits are pseudo-carry bits.

11. (Original) The apparatus as recited in claim 10, wherein each of said subset of said plurality of summation units is configured to generate said plurality of sum bits in response to receiving a propagate bit and a corresponding one of said pseudo-carry bits.

12-22 (Cancelled)

23. (New) The apparatus as recited in claim 7, wherein another subset of said plurality of summation units is configured to generate another portion of said plurality of sum bits in response to receiving a different carry bit.

24. (New) The apparatus as recited in claim 7, wherein each generate and propagate bit pair occupies an ordered position from a least significant ordered position to a most significant ordered position.

25. (New) The apparatus as recited in claim 24, wherein each of said ordered plurality of carry bits occupies an ordered position from a least significant ordered position to a most significant ordered position.

26. (New) The apparatus as recited in claim 25, wherein each of said ordered plurality of carry bits is based upon all generate and propagate bit pairs occupying less significant ordered positions.

27. (New) The apparatus as recited in claim 8, wherein another subset of said plurality of summation units is configured to generate another portion of said plurality of sum bits in response to receiving a different carry bit.

28. (New) The apparatus as recited in claim 8, wherein each generate and propagate bit pair occupies an ordered position from a least significant ordered position to a most significant ordered position.

29. (New) The apparatus as recited in claim 28, wherein each of said ordered plurality of carry bits occupies an ordered position from a least significant ordered position to a most significant ordered position.

30. (New) The apparatus as recited in claim 29, wherein each of said ordered plurality of carry bits is based upon all generate and propagate bit pairs occupying less significant ordered positions.